

# List of to knows for VLSI

## \* CMOS

P channel  
N channel  
cross sections  
Current Voltage characteristics.  
NAND, NOR, complex CMOS designs.

## \* Verilog Programming

## \* Static Ram

Unit cell  
Array configuration

## \* Dynamic Ram

Charging discharging/refresh time  
Cross sectional area  
Array configuration  
Unit cell

## \* ROM

Charge of threshold voltage  
Array configuration

## \* PROM

Cell  
how to write to cell  
know that it can only be used once.

## \* EPROM

Cell  
Array  
Cross sectional array (double dielectric)  
to write and clear  
Energy band diagram

## \* EEPROM

floating gate (quantum tunneling)  
Cross sectional area.  
Energy band diagram  
Change of threshold voltage due to FG.  
Symbol  
Cell / Array  
How to write / clear

## \* Flash EEPROM

Cross sectional area  
Symbol  
Cell / Array  
How to write clear  
Main difference b/t EEPROM

## \* Logic Circuits

Steps to logic circuit design

## \* Half adder

Steps to logic design (Derived fr TTAB)

## \* Full adder

Truth Table  
Steps of design

## \* PLA (Double Array)

Know how to make connections.

## \* PAL (Single Array)

Know how to make connections.

## \* FPGA

How to make connections to FPGA.



- \* Design w 2-1 multiplexers (Combination logic)  
How to design w 2-1 multi.
- \* Multiplexer / Demultiplexer  
Truth table and design of each.
- \* Decoder / Encoder  
Truth table and design
- \* Cool Converters  
7 seg display design.

- \* SR Latch  
Truth table  
Operation  
Gated SR Latch  
2 designs
- \* D latch  
2 designs  
Similarity with SR latch  
Operation

- \* T flip flop  
Similarity with D latch schematic.

- \* JK Flip flop  
Truth table, similarities w TFF

- \* Registers  
Parallel  
Series  
Series / Parallel

- \* Counters  
Circuit (?)

## \* Processor

Block Diagram (i/c registers/bus lines  
/buffer/ALU/  
~~controller~~  
control unit)

## \* Control unit register

Design w multiplexers

## \* Digital System Design

\* Steps for sync machine

\* Steps for a-sync machine